REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for notice that Claims 2-13, 22 and 23 are allowable.

Applicants have amended the Specification to correct various informalities. Furthermore, Applicants have amended Claims 14-15 and 18-20. Claim 20 has been amended to provide proper antecedent basis within the claim. Claims 14-15 and 18-19 have been amended such that the limitation "compressed" modifies each instance of "transport stream." Applicants respectfully submit that the addition of the term "compressed" to the aforementioned claims expressly delineates that which was inherently present in the claimed invention. Applicants draw the Examiner's attention to the Specification. Page 1, lines 16-17 states, "[t]he compressed MPEG-2 format is referred to as a transport stream." Furthermore, page 6, lines 5-7 states, "the HDTV transport stream received by the capture block 310 of Figure 4 . . . is a compressed video stream, such as MPEG 2."

Lastly, Claim 18 has been amended to clarify and provide proper antecedent basis with the Specification in accordance with 35 U.S.C. § 112, ¶ 2. As a result, the term "system interface port" has been replaced with the limitation "bus interface port coupleable to a central processing unit." In support of the amendment, Applicants respectfully draw the Examiner's attention to page 5, lines 25-29 of Applicants' Specification and Figure 2, elements 230 and 250. Similarly, the term "video engine" has been replaced with the limitation "engine operative to decompress the compressed transport stream." Applicants draw the Examiner's attention to page 15, lines 3-4 for antecedent basis. Additionally, Applicants have clarified the express limitation of receiving a compressed transport stream by amending the claim to include that which was inherently present as filed. In so doing, Applicants have added language indicating that the video graphics adapter "having an input to receive the compressed transport stream." (See Figure 2, element 230 indicating the manner in which the transport stream enters the video adapter). Applicants respectfully submit that no new subject matter has been added in the aforementioned amendments.

Claims 14-17 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cheney et al., U.S. Patent No. 6,519,283 ("Cheney") in view of Adams et al., U.S. Patent No. 6,108,042 ("Adams"). With respect to Claim 14, Applicants respectfully submit that Cheney is directed toward an integrated digital video system configured to implement picture-in-picture ("PIP") merging of video signals from two or more video sources as well as selective overlapping of on-screen display graphics onto the resultant merged signal. (See Abstract.) The reference explains that a first picture of the PIP display is received as a digital video signal from a satellite or cable in the form of a compressed transport stream. (Col. 6, lines 35-39; Figure 4, element 104).

The Office Action cites Cheney for teaching "receiving a compressed transport stream associated with a digital video broadcast signal, the compressed transport stream having data signals and control signals." Specifically, the Action notes that Cheney discloses the input of an analog or secondary digital video stream, vis-à-vis, an external graphics/video port (EGV) wherein the EGV port includes a receiver/driver circuitry for accommodating in parallel a plurality of input/output signals, including *pixel data signals* and corresponding *synchronization signals*. (Col. 4, lines 40; lines 55-57; emphasis added). However, Applicants respectfully note that the reference explains that the EGV port is utilized to receive uncompressed video signals from a second video source to implement and display the other/second picture in the PIP display. (Col. 6, lines 57-67). Therefore, while the signals provided as input to the EGV port are digital, they are uncompressed and therefore not analogous to the claimed "compressed transport stream associated with digital video broadcast signals."

Applicants respectfully note that by not teaching a compressed transport stream having data signals and control signals, Cheney cannot disclose or teach the step of "generating a secondary set of control signals from the compressed transport stream's control signals" or the step of "storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary set of control signals."

For arguments sake, however, Applicants respectfully note that while the Office Action cites the frame buffer pointer control (Cheney, Figure 6, Element 6a) as rendering obvious "a secondary set of control signals," the Office Action appears to be silent as to the origin of the

secondary set of control signals. Claim 14 requires, among other things, that the secondary set of control signals are generated *from* the compressed transport stream's control signals.

Because Cheney does not appear to teach Applicants' step of "receiving a compressed transport stream . . . having data signals and control signals," and further does not appear to teach the step of "generating a secondary step of control signals from the compressed transport stream's control signals," Applicants submit that Cheney does not disclose the step of "storing at least a portion of the compressed transport stream data signals in a memory buffer controlled by the secondary step of secondary set of control signals." As a result, Applicants respectfully believe that Cheney does not disclose, teach or suggest any of the limitations contained within Claim 14.

With respect to the final limitation of Claim 14, i.e., "sending the content to the memory buffer to a system bus," the Office Action cites the Adams reference as teaching a graphics display system (Figure 2, element 56), which includes a frame buffer that may send information to the system bus (Figure 2, element 51). Applicants respectfully note that while Figure 2 shows the graphics display subsystem coupled to the system bus, the reference teaches that the processor 52 communicates with the memory subsystem, the graphics display subsystem, the data modem, the disk drive, and the audio subsystem via system bus 51. (Col. 5, lines 29-32). The reference continues to teach that the graphics display subsystem performs graphics-rendering functions and includes a frame buffer and associates circuitry to *drive the display device* (Figure 2, element 12). (Col. 5, lines 41-43; emphasis added). For the aforementioned reasons and because Adams appears to be silent as to the sending of transport stream data to a system bus, Applicans suggest that Adams only teaches the method of sending the contents of a memory buffer in the direction of the display and not in the direction of the system bus. As a result, Adams does not appear to disclose the step of "sending the contents of the memory buffer to a system bus" wherein the contents of the memory includes, among other things, at least a portion of the transport stream data signals.

Applicants respectfully note that no combination of Cheney or Adams teach or suggest Applicants' claimed invention. As such, Applicants respectfully believe that Claim 14 is in proper condition for allowance.

With regard to Claim 15, Applicants respectfully repeat the relevant remarks made above with respect to Claim 14. Specifically, Applicants note that Cheney is silent as to the steps of "receiving a transport stream...*having data signals and control signals*, generating a secondary set of control signals *from the transport streams control signals*, and storing at least a portion of the transport stream data signals in a memory buffer controlled by the secondary set of control signals." (Claim 14, emphasis added). By receiving an uncompressed digital video signal (associated with the second picture of a PIP display) containing pixel and synchronization signals in an EGV Port, the Cheney reference appears to teach the step of "receiving a digital video signal having data signals and control signals, wherein the digital video signal is of a different type than the compressed transport stream" as required by Claim 15. The reference, however, does not appear to teach the step of "generating the secondary set of control signals from the digital video signal's control signals" and "storing at least a portion of the digital video signals in the memory buffer based on the secondary set of control signals." Moreover, while the Office Action makes reference to the pixel select control signals of Column 7, lines 40-41, as teaching the control signals associated with the transport stream, Applicants respectfully note that the signals appear to be generated by a processor and not contained within a digital video signal. (Col. 7, lines 22-27). For the aforementioned reasons, Applicants respectfully believe Claim 15 to be in condition for allowance.

With respect to Claim 16 and 17, Applicants respectfully repeat the relevant remarks made above with respect to Claim 14 and Claim 15. Because Claims 16 and 17 depend upon allowable base Claim 14 and further contain patentable subject matter, Applicants respectfully believe the claims to be allowable over Cheney and Adams.

Claims 18-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Reitmeier, U.S. Patent No. 6,118,498, ("Reitmeier") in view of Schindler, et al., U.S. Patent No. 5,900,867, ("Schindler"). With respect to Claim 18, Applicants respectfully note that the Reitmeier reference fails to teach or suggest the claim limitation of "a video graphics adapter having an input to receive the compressed transport stream . . . the video graphics adapter further includes a bus interface port coupleable to a central processing unit." Applicants respectfully submit that neither the format converter (Figure 2, element 50) nor the controller (element 70) is analogous to a video graphics adapter. It contrast, it appears that the format converter merely

comprises a video decoder and display frame buffer and does not include "a bus interface port coupleable to a central processing unit." Moreover, the controller does not receive a compressed transport stream, or include a bus interface port, video engine or video output port.

While the Office Action states that the "system interface port F, which connects to controller 70 through I/O port 72" teaches Applicants' claimed invention of a "bus interface port," Applicants respectfully note that signal F appears to be merely a control signal originating from the I/O port of the controller and terminating at the format converter. Reitmeier teaches that the control signal F, when sent, instructs the format converter to operate in a pass-through mode. (Figure 1; Col. 4, lines 53-55). Figure 2 illustrates a unidirectional control signal that appears to be sent along a pin-to-pin connection in contrast to a bus, which by definition operates in a bi-directional manner along a multiple pin connection. Furthermore, Applicants submit that unidirectional 'data channel' along which the control signal F is sent does not transmit data and address information as those of ordinary skill in the art expect in a bus.

Moreover, while Applicants submit that Reitmeier does not teach a video graphics adapter, Applicants respectfully note, for argument's sake, that the input/output port is part of the controller (element 70) and therefore not contained within the format converter or any video graphics adapter as required by Claim 18. Claim 18 requires, among other things, a video graphics adapter that includes a bus interface port coupleable to a central processing unit. Applicants respectfully submit that neither the format converter (element 50) nor any part thereof is coupleable to the controller (element 70) or its CPU (element 74). As a result, Reitmeier does not appear to teach or suggest any of Applicants' Claim 18.

With respect to the Schindler reference, Applicant's respectfully note that while Schindler discloses a video graphics adapter and a PCI Bus (Figure 5), Applicants respectfully note that Schindler teaches away from the claimed invention. Schindler teaches that the video graphics adapter card as described in Figure 5 is coupled to the PCI Bus *to receive* MPEG encoded video. The reference teaches the controller 510 detects MPEG data on the PCI Bus and routes it to a decoder which decodes the MPEG data in accordance with MPEG standards. (Column 11, lines 34-41). In contrast, Applicants claim "a video graphics adapter having an input to receive the compressed transport stream, the video graphics adapter further includes a

bus interface port coupleable to a central processing unit." (Emphasis added). Applicants respectfully submit that the claimed invention delineates between a separate and unique input port designated as "an input to receive the compressed transport stream" and another port designated as "a bus interface port coupleable to a central processing unit." Because Schindler does not discriminate between more than one port in the manner claimed by Applicants, Applicants submit that Schindler fails to teach "a video graphics adapter having an input to receive the compressed transport stream" wherein the input of the video graphics adapter is structurally separate from the bus interface port.

As a result of the foregoing remarks, Applicants respectfully contend that no combination of Reitmeier or Schindler disclose Applicants' claimed invention. Applicants believe Claim 18 to be in proper condition for allowance.

With respect to Claims 19 and 20, Applicants respectfully repeat the relevant remarks made above with respect to Claim 18 and further note that both claims recite patentable subject matter. As a result, Applicants also believe Claims 19 and 20 to be in proper condition for allowance.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Cheney, in view of Malladi et al., U.S. Patent No. 6,519,283, ("Malladi"), and in further view of Datari, U.S. Patent No. 6,418,169, ("Datari").

With respect to Claim 21, the Office Action cites Cheney for teaching Applicants' step of "in a first mode of operation, storing pixel information in a frame buffer of a vide adapter." While Cheney appears to teach receiving of an uncompressed analog or secondary digital video stream for use as the second display of a PIP system, Cheney does not appear to teach storing pixel information in a frame buffer of a video adapter. In contrast, the Office Action's citation to Column 5, line 52-Column 6, line 6, is in reference to the storage of pixel data, but rather the storage of MPEG encoded data. Cheney teaches that "MPEG encoded video data is fetched from PCI bus by a DMA controller which writes the data to a video [FIFO] buffer." (Column 5, Lines

56-58). Moreover, Applicants respectfully repeat the relevant remarks made above confirming the Office Action's admission that Cheney fails to teach a video adapter. As a result, Applicants respectfully believe that Cheney fails to teach Applicants' claim limitation requiring, among other things, "storing pixel information in a frame buffer of a video adapter."

Because no reference teaches or suggests Applicants' limitation directed toward storing pixel information in a frame buffer of a video adapter, Applicants respectfully submit that Claim 21 has not been rendered obvious. For argument's sake, however, Applicants note that Malladi appears to teach away from Applicants' claimed invention. While Malladi generally deals with the storage of decompressed MPEG data (i.e., pixel data) and further appears to store the pixel data on a scan line basis, Malladi does not teach "storing pixel information in a frame buffer of a video adapter." In fact, Malladi does not appear to teach or suggest a video adapter. Applicants note that the reference appears to be directed primarily at an MPEG decoder block. In any event, Applicants respectfully draw the Examiner's attention to Column 4, lines 16-17 which state, "[t]he MPEG decoder also includes *an external memory* which stores prior decoded reference [pixel] frames." (See Column 4, lines 37-40 defining a reference frame as containing pixel data; See element 204 of Figure 5). By failing to teach or suggest a video decoder and by only describing an *external* memory, Applicants respectfully submit that Malladi does not teach or suggest Applicants' Claim 21.

With respect to Applicants' limitation including "in a second mode of operation, storing compressed transport stream data in a frame buffer, wherein one line of the frame buffer memory is representative of one transport stream packet," Applicants respectfully repeat the relevant remarks made above noting that Cheney does not teach a video adapter. As a result, Applicants note that while Cheney appears to teach the receiving and storage of a compressed transport

stream, Cheney fails to teach or suggest Applicants' claimed invention which requires, among other things, "storing compressed transport stream data in the frame buffer" wherein the frame buffer is "of a video adapter" as previously delineated in Claim 21 and referenced by Applicants' use of the article "the" modifying "frame buffer."

Moreover, and with respect to the Datari reference, Applicants respectfully submit that storing MPEG packets "in memory and sequentially access[ing] in accordance with a predetermined priority profile (map) associating data having a specific characteristic and function with a desired priority" as cited by the Office Action (Col. 5, Lines 25-42) is not analogous to Applicants' claimed invention. Applicants claim "storing compressed transport stream data in a frame buffer, wherein one line of the frame buffer memory is representative of one transport stream packet." Applicants respectfully note that the cited Datari reference merely discusses that MPEP packets are stored in memory. Datari gives no indication of the manner in which the packets are stored (i.e., the reference does not teach or suggest storing "wherein one line of the frame buffer memory is representative of one transport stream packet"). The reference only indicates how data is accessed.

For the aforementioned reasons, Applicants respectfully believe Claim 21 to be in proper condition for allowance.

Accordingly, Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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